EELE 261 Cheat Sheet:

# Chapter 7

## Section 1:

## Section 2: Sequential Logic timing considerations

Timing specifications for sequential storage devices:

-setup time; tsetup (ts): the setup time specifies how long the data input needs to be at a steady state *before* the clock event.

-hold time; thold (th): specifies how long the data input needs to be at a steady state *after* the clock event.

-metastable time; tmeta : the time a storage device will remain metastable

- Clock-to-Q; tCQ : delay from the time a clock transition occurs to the point that the data is present on the Q output.

-If these specifications are violated, the storage device will be unable to determine whether the input was a 0 or a 1 and will go metastable.

## Section 3: Common Circuits Based on Sequential Storage Devices